# DC Imperfections
Offset Voltage

- The IC Op-amp comes so close to ideal performance that it is useful to state the characteristics of an ideal amplifier without regard to what is inside the package.

  - Infinite voltage gain
  - Infinite input impedance
  - Zero output impedance
  - Infinite bandwidth
 - Zero input offset voltage (exactly zero out if zero in).

- Build any op amp circuit, apply zero voltage to its input, and what do you expect at the output?

- Although you would zero voltage, there is actually an error voltage present at its output.

- What causes this error? You can trace the error back to a number of unbalances in the op amp's internal transistors and resistors. To account for this in a circuit design, the net error is **modeled** as an offset voltage, V_{OS}, in series with op amp's input terminals.

- How will it affect the circuit? That depends on the op amp itself and the circuit design.

- The input offset voltage can range from µV to mV and can be either polarity.

- Bipolar op amps have lower offset voltages than JFET or CMOS types.

- The offset voltage is modeled in series with one of the op amp input terminals. Which one?

- Although the net effect is the same at either input, it is much easier to analyze V_{OS} in series with the non-inverting input. Why? The resulting circuit with V_{OS} at V+ looks just like the **non-inverting amplifier** configuration.

R2

R1

-

V_{OS}

+

V_o
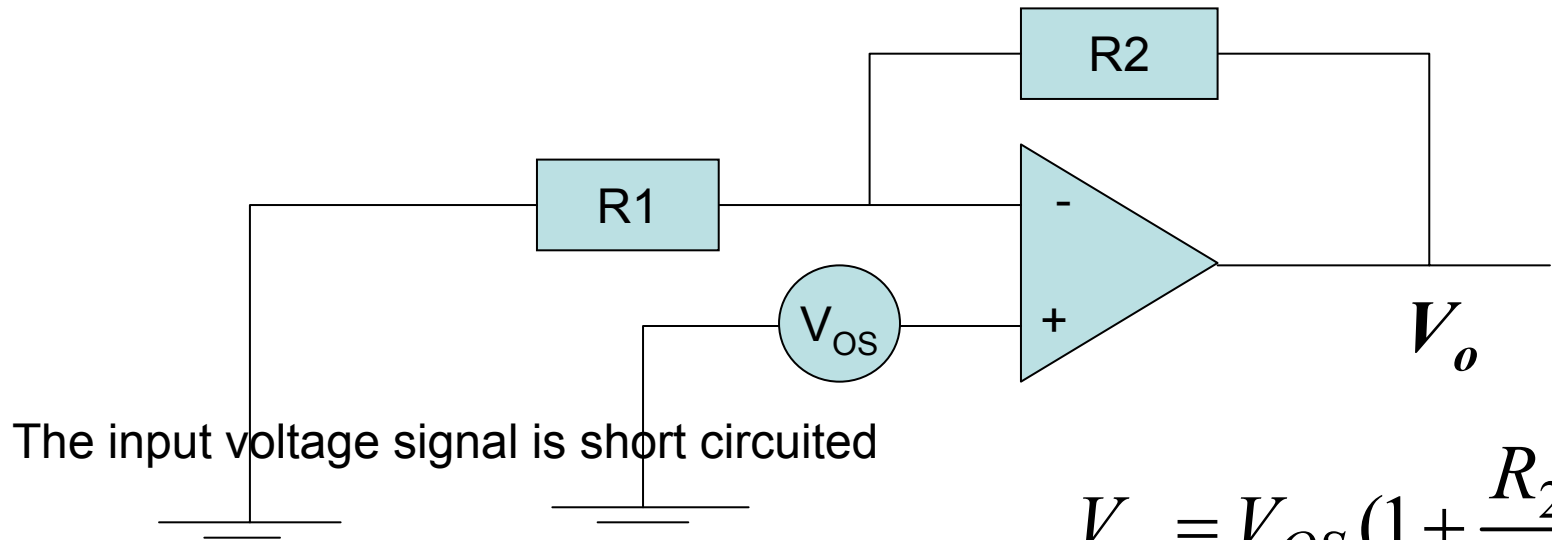
The input voltage signal is short circuited

$$V_o = V_{OS}(1 + \frac{R_2}{R_1})$$

Actual op amp

-

+

- +

Offset free op amp

V_{OS}
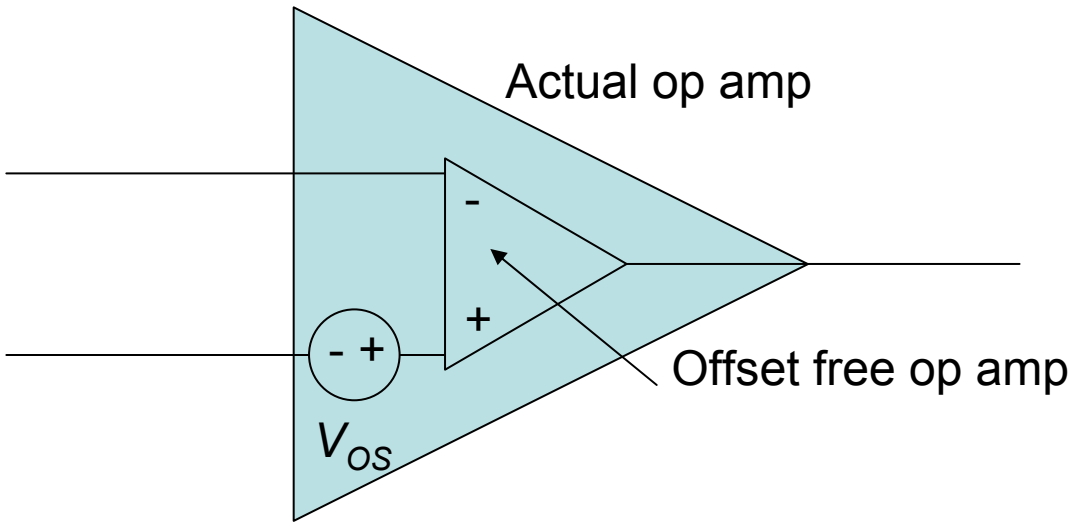
Offset Voltage Compensation

- In many applications, especially those for which the input signal is large compared to the offset voltage V_{OS}, the effect of the offset voltage is negligible.

- However, there are situations in which it is necessary to compensate for or null out the offset voltage.

- Two such methods are:
  - **Offset null terminals:** Some op amp are provided with two additional terminals to which a specified circuit can be connected to trim to zero the output DC voltage due to V_{OS}.
  - Offset compensation circuit through two terminals.
  - Capacitively coupling the amplifier.

V+

V-

Offset nulling
terminals
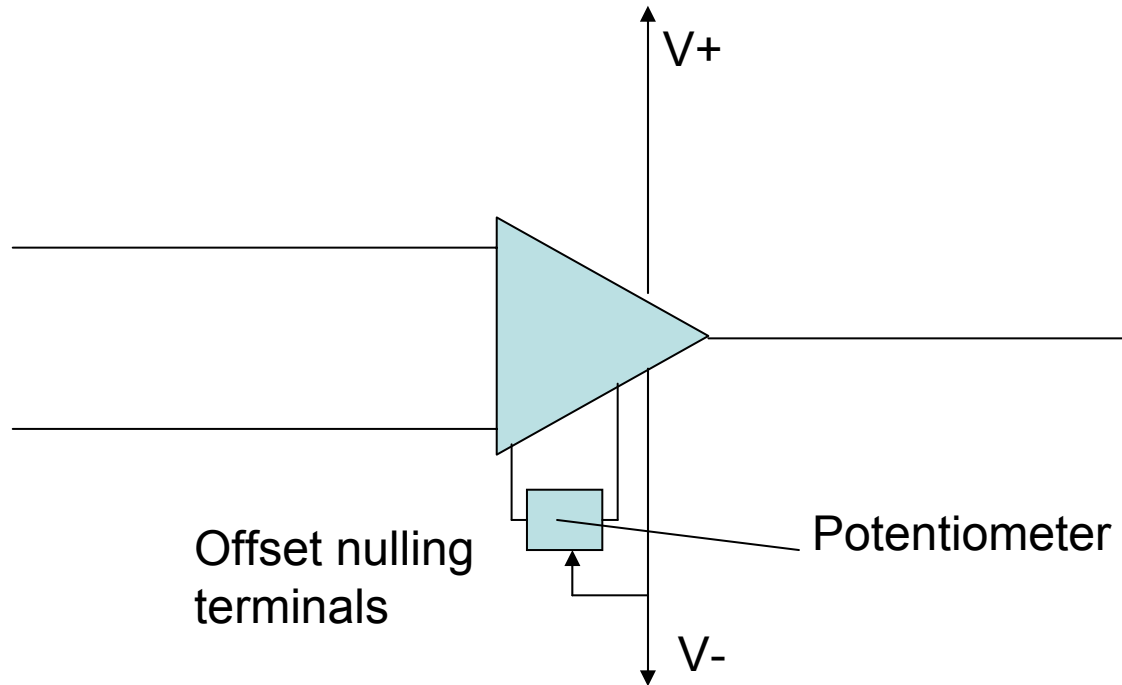
Potentiometer

The output DC offset voltage of an op amp can be trimmed to zero by
Connecting a potentiometer to the two offset-nulling terminals. The wiper
Of the potentiometer is connected to the negative supply of the op am.
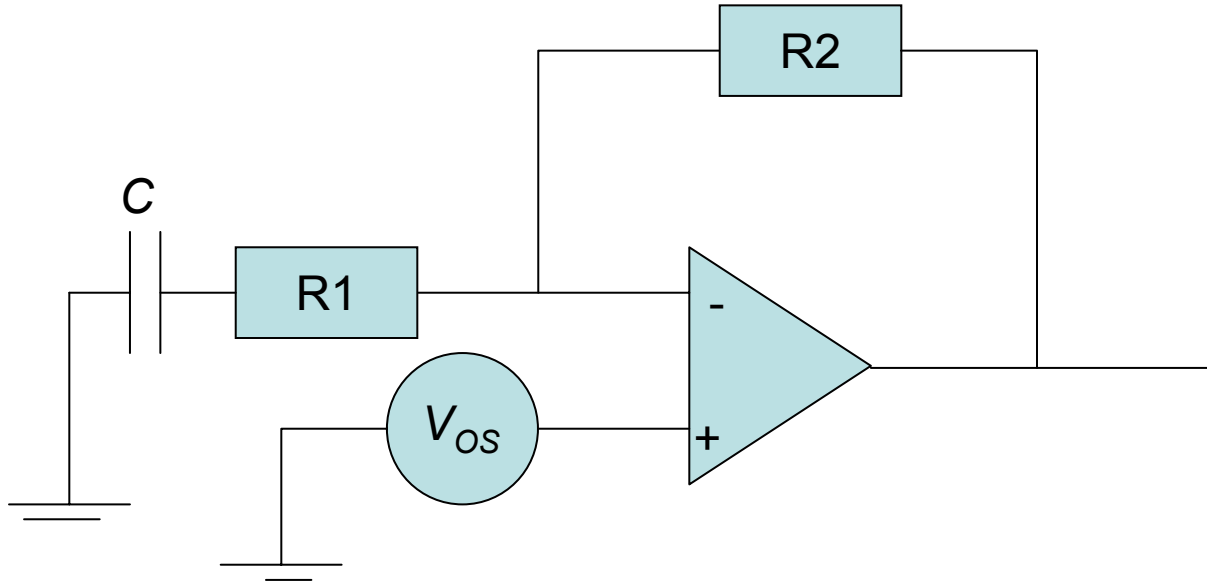
Capacitively coupled inverting amplifier.

Exercise 2.24: Consider an inverting amplifier with a nominal gain of 1000 constructed from an op amp with an input offset voltage of 3 mV and with output saturation levels of ±10 V. (a) What is the peak sine-wave input signal that can be applied without output clipping? (b) If the effect of V_{OS} is nulled at room temperature (25 oC) how large an input can now one apply if: (i) the circuit is to operate at a constant temperature? (ii) the circuit is to operate at a temperature in the range 0°C to 75 °C and the temperature coefficient of V_{OS} is 10 μV/°C?

$$V_O = V_{OS}(1+\frac{R_2}{R_1}); \ V_O = 3\text{mV}(1+1000) = 3 \text{ V}$$

Maximum amplitude of a sine wave at the op amp output is $10 - 3 = 7\text{V}$.

(b) For part (i) $= 10 \text{ mV}$

(b) For part (ii) : Temperature range of 0^OC to 75^OC corresponds to input offset voltage range of $(0 - 25) \times 10\mu\text{V} = -250\mu\text{V}$ to $((75 - 25) \times 10\mu\text{V} = 500\mu\text{V}$.

This input offset range corresponds to output DC levels of

$-250\mu\text{V}(1+1000) = -0.25 \text{ V}$ to $500 \ \mu\text{V} \ (1+1000) = 0.5 \text{ V}$.

Exercise 2.25: Consider an inverting amplifier with a nominal gain of 1000 constructed from an op amp with an input offset voltage of 3 mV and with output saturation levels of ±10 V. The amplifier is capacitively coupled. (a) What is the DC offset voltage at the output and what is the peak sine wave signal that can be applied at the input without output clipping? Is there a need for offset trimming? (b) If $R_1 = 1$ kΩ and $R_2 = 1$ MΩ, Find the value of C that will ensure that the gain will be greater than 57 dB down to 100 Hz.

The maximum amplitude of a sine wave at the output without clipping is

10 - 0.3 mV = 9.997 V, accordingly there is no need for offset trimming.

(b) The magnitude of the gain of this amplifier is $|A_d| = \dfrac{R_2}{\left|R_1 + \dfrac{1}{j\omega c}\right|} = \dfrac{R2}{\sqrt{R_1^2 + \dfrac{1}{c^2\omega^2}}}$

$20\log|A_d| \rangle 57; \quad |A_d| \rangle 707.95;$

$\dfrac{R2}{\sqrt{R_1^2 + \dfrac{1}{c^2\omega^2}}} \rangle 707.95; C = 1.59\,\mu F$

Op-amp Input Offset Current

- One of the practical op amp limitations is that the input bias currents for the two inputs may be slightly different.

- Even though the inputs are designed to be symmetrical, slight differences which occur in the manufacturing process may give slightly different bias currents.

- This offset current is typically on the order of a tenth of the input bias current, with 10 nA being a representative offset current for a 741 op amp.

- Even with identical source impedances, this offset current will produce a slight voltage between the input terminals, contrary to the ideal op amp.

R_2

$I_{B1} - I_{B2}R_3/R_1$

$I_{B2}R_3/R_1$

R_1

0 V

I_{B1}

I_{B2}

R_3

+

I_{B2}

V_o
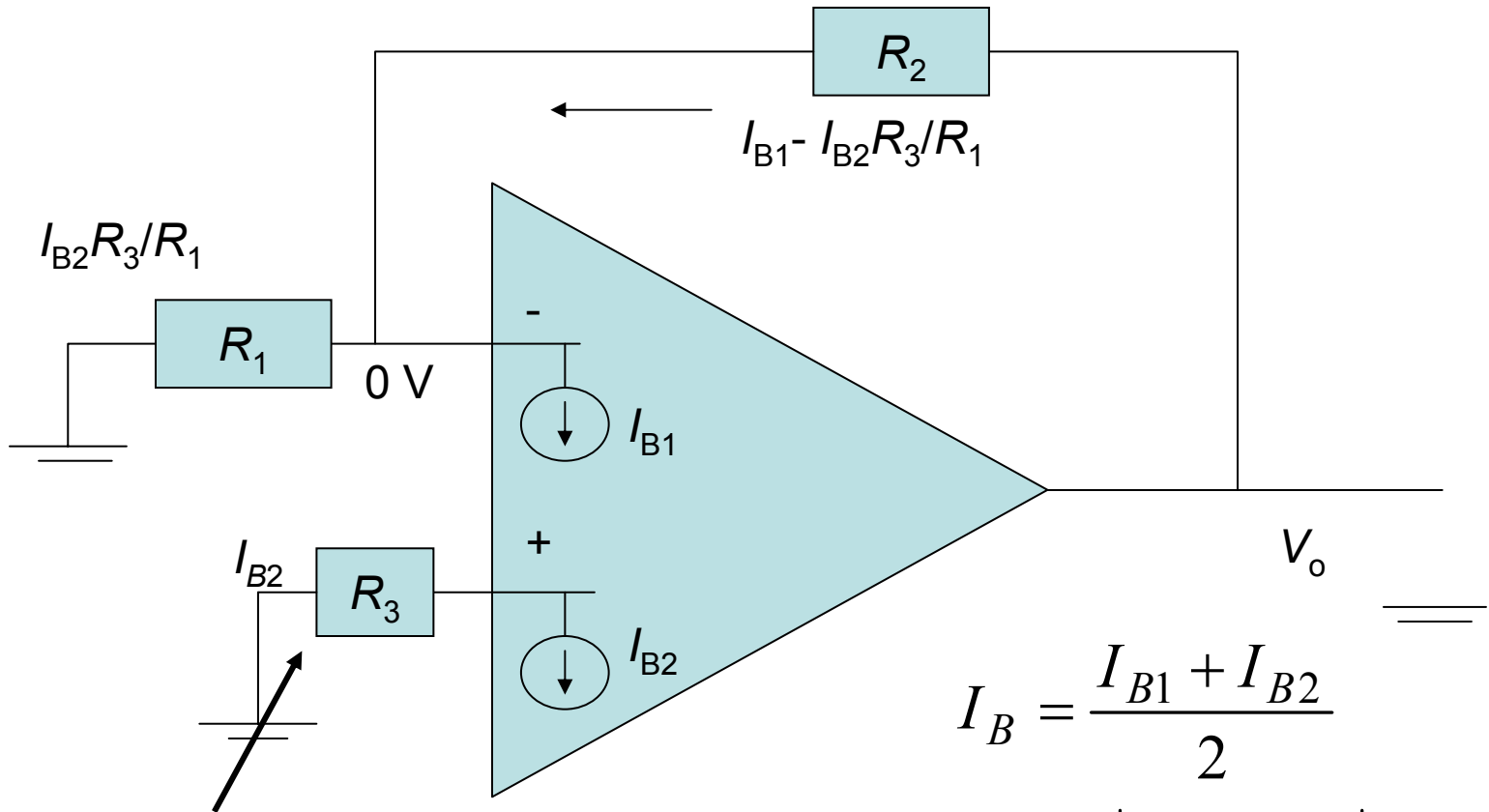
A resistor may be added in series with the
Non-inverting input lead to reduce the value of
The output dc voltage due to input bias currents

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

$$I_{OS} = \left| I_{B1} - I_{B2} \right|$$

$$V_o = I_{B1}R_2 \approx I_B R_2 \ (\text{no } R_3)$$

$$V_o = I_{OS}R_2 \ (\text{with } R_3)$$

$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

- To minimize the effect of the input bias currents one should place in the positive lead a resistance equal to the DC resistance seen by the inverting terminal.

- If the amplifier is AC coupled, we should select $R_3 = R_2$.

- We must always provide a DC path between each of the input terminals of the op amp and ground. If we couple both input of the amplifier then the circuit will not operate without the resistance R_3 to ground.

2.26: Consider an inverting circuit designed using an op amp and two resistors, R_1 = 10 kΩ and R_2 = 1 MΩ. If the op amp is specified to have an input bias current of 100 nA and an input offset current of 10 nA, find the output DC offset voltage resulting and the value of resistor R_3 to be placed in series with the positive input lead in order to minimize the output offset voltage. What is the new value of Vo.

$$V_O = I_B R_2 = 100\,\text{nA} \times 1\,\text{M}\Omega = 0.1\,\text{V}$$

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} = 9.9\,\text{k}\Omega \approx 10\,\text{k}\Omega$$

$$V_O = I_{OS} R_2 = 10\,\text{nA} \times 9.9\,\text{kA} \approx 0.01\,\text{V}$$