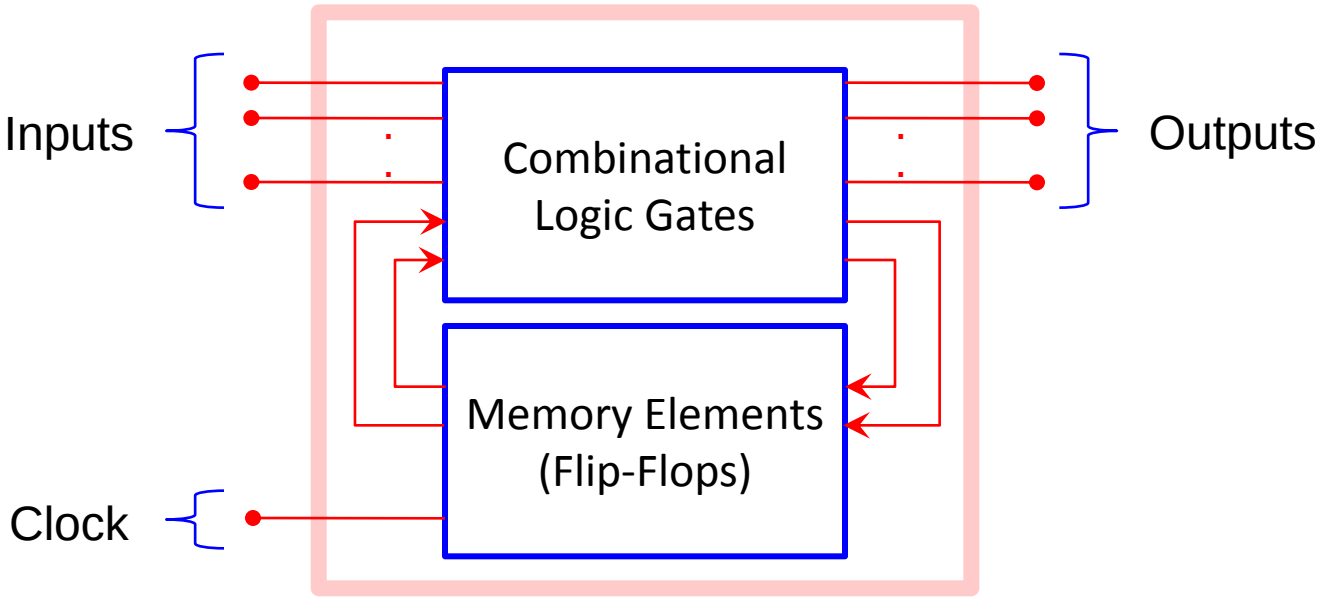
Sequential Logic and The Flip-Flop

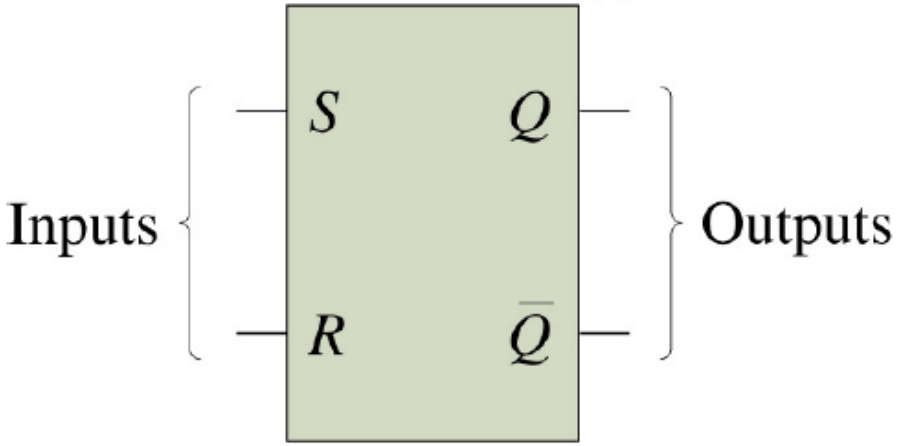
Sequential logic may have one or more, inputs and one or more outputs. However, the outputs are a function of both the present value of the inputs and also the previous output values. Sequential logic requires memory to store these previous outputs values.

Sequential circuit = Combinational logic + Memory Elements



Latches and Flip Flops

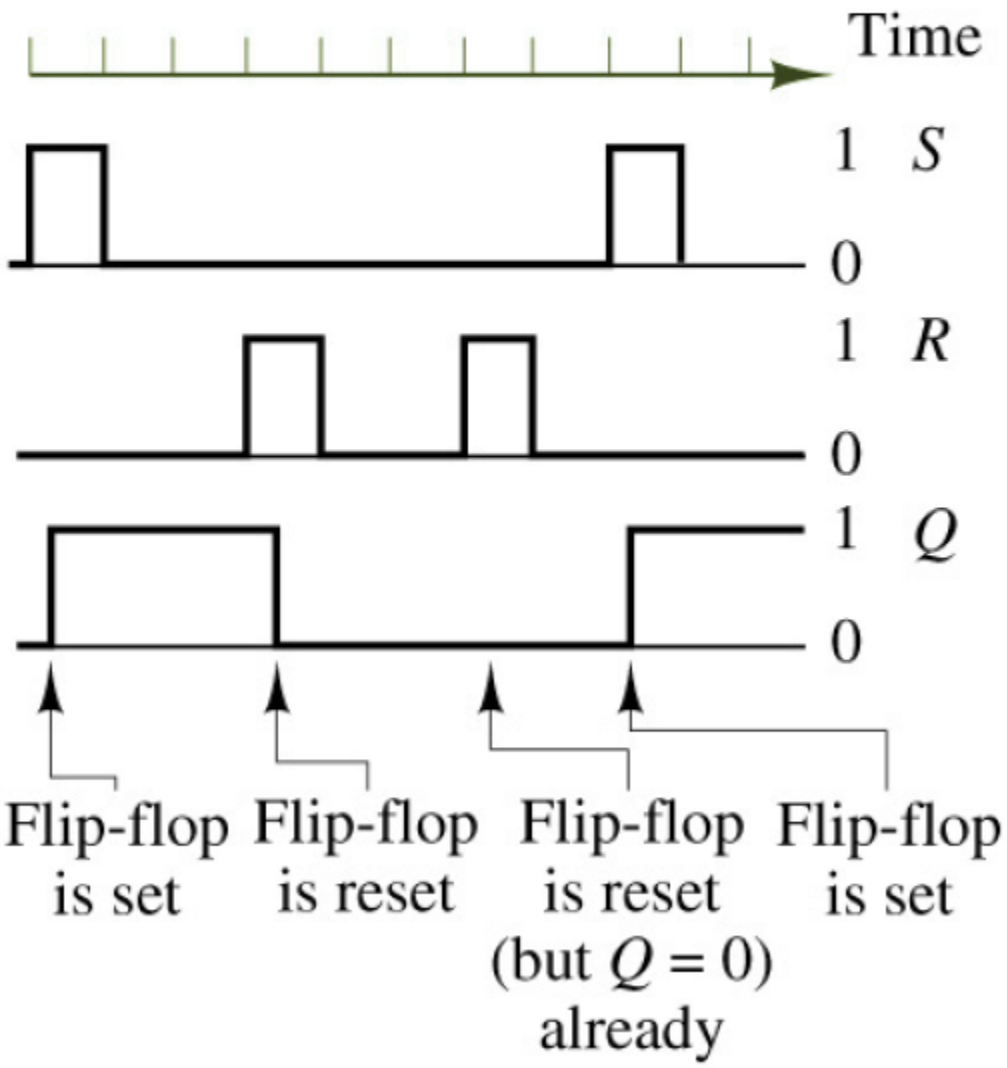
- A Flip-flop is a bistable device, that is, it can remain in one of two states (0 or 1) until appropriate conditions cause it to change state. Therefore, a flip-flop can serve as a memory element.
- A flip-flop has two outputs, one of which is the complement of the other.
- For example, *RS* flip flop has two inputs (*R* and *S*) and two outputs . When *R* = *S* = 0, the *SR* flip flop remains in its present state.
- When *S* = 1 and *R* = 0, the *RS* flip flop is set to 1 state.
- When *S* = 0 and *R* = 1, the SR flip flop is reset to 0.
- It is not permitted for both *S* and *R* to be equal to 1.



S	R	Q
0	0	Present state
0	1	Reset
1	0	Set
1	1	Disallowed

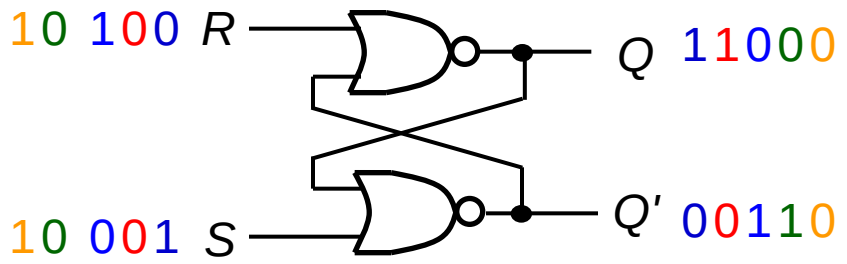
Timing diagram for the *RS* flip-flop

S	R	Q
1	0	1
0	0	1
0	0	1
0	1	0
0	0	0
0	0	0
0	1	0
0	0	0
1	0	1
0	0	1



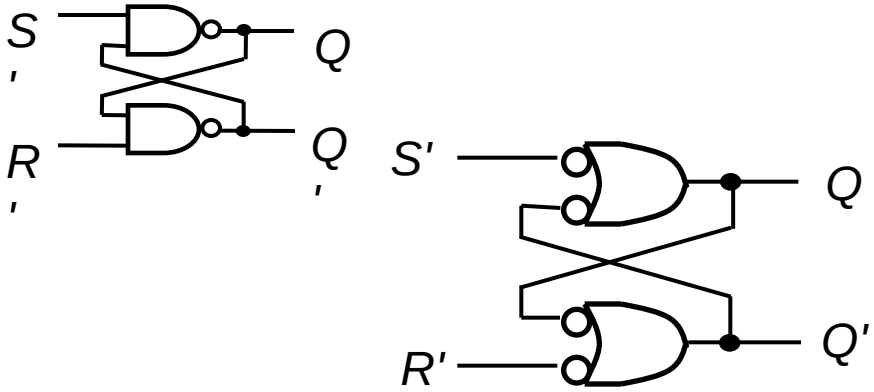
S-R Latch

- Active-HIGH input S-R latch



S	R	Q	Q'	
1	0	1	0	initial
0	0	1	0	(afer S=1, R=0)
0	1	0	1	
0	0	0	1	(after S=0, R=1)
1	1	0	0	invalid!

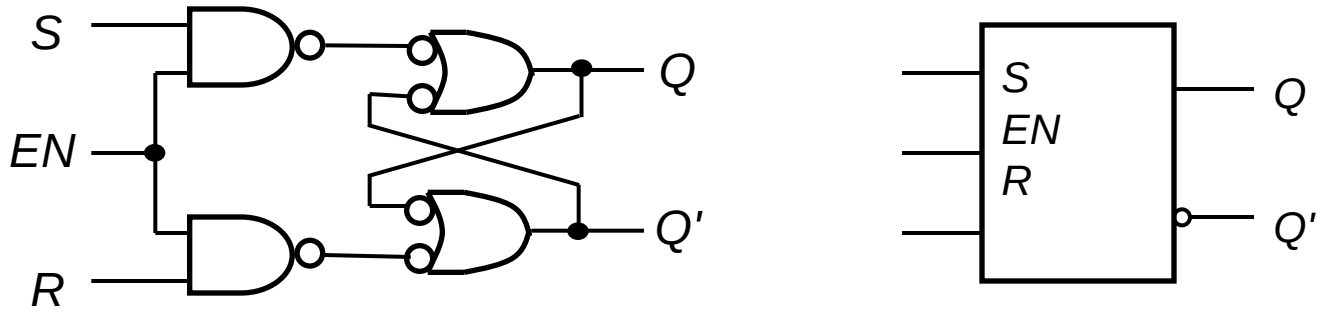
- Active-LOW input S'-R' latch



S'	R'	Q	Q'	
1	0	0	1	initial
1	1	0	1	(afer S'=1, R'=0)
0	1	1	0	
1	1	1	0	(after S'=0, R'=1)
0	0	1	1	invalid!

Gated *S-R* Latch

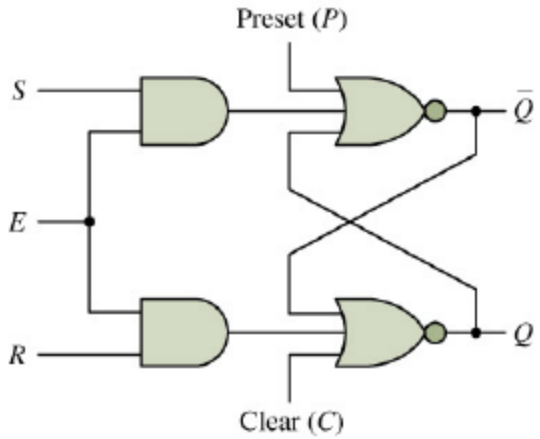
S-R latch + *enable input* (*EN*) and 2 NAND gates → *gated S-R latch*.



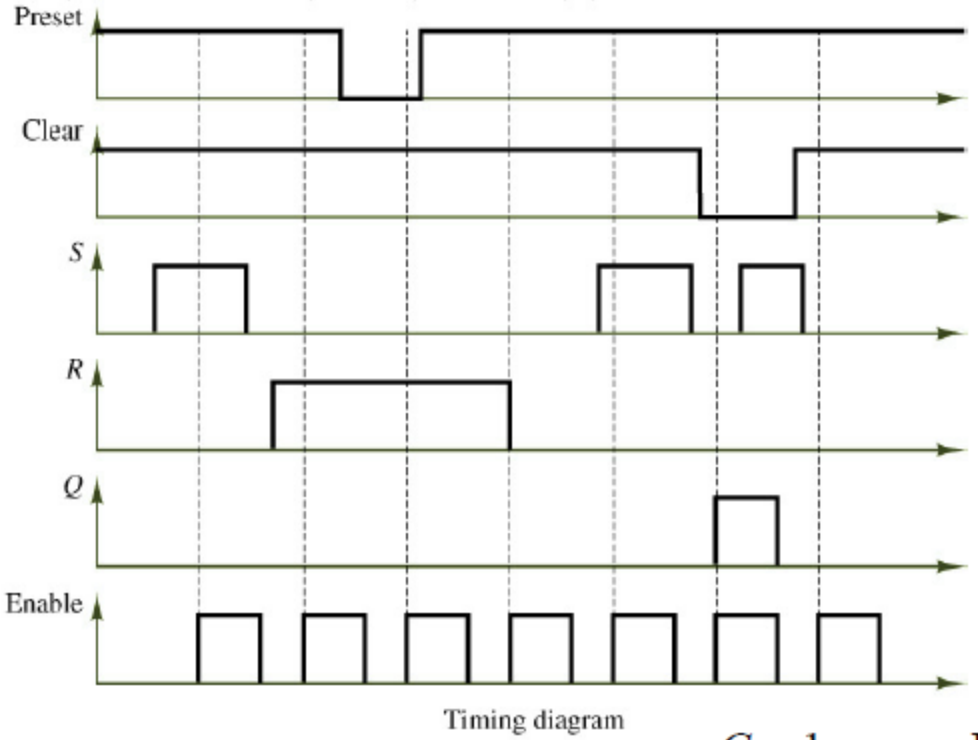
When the Enable is high the circuit acts as a conventional active high input S-R latch
But when the enable is low the circuit ignores any signal applied to the S-R inputs.

$P = 1$ means $S = 1$

Clock



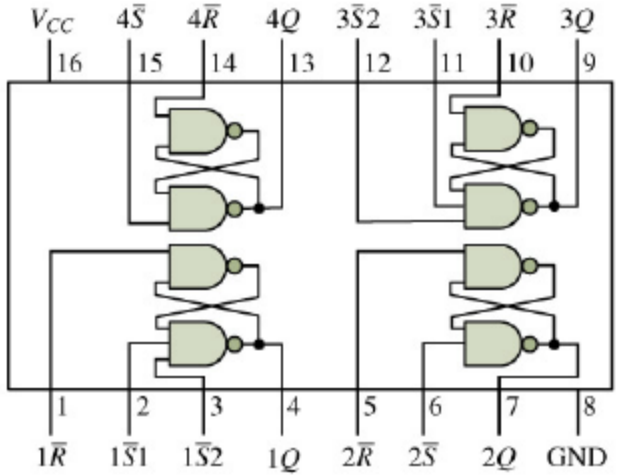
(a)



Timing diagram

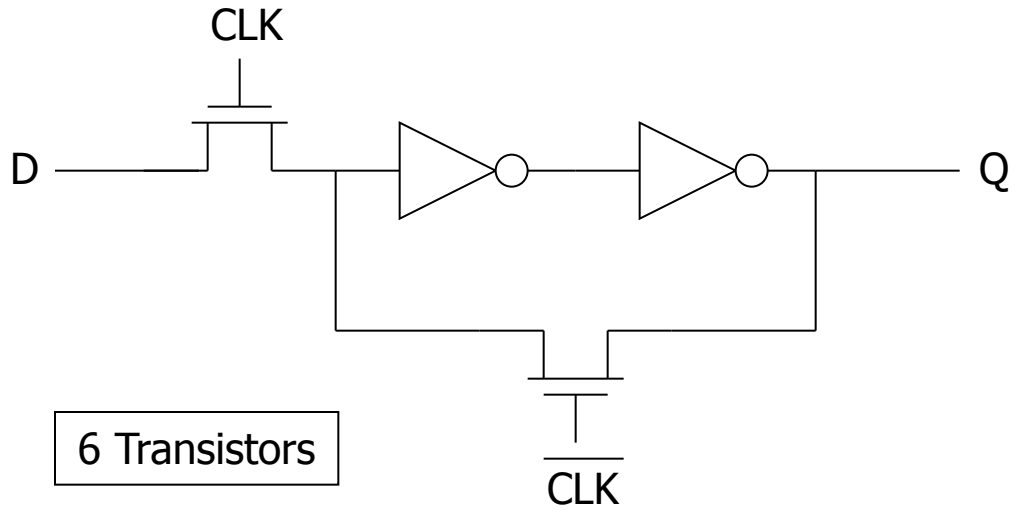
(b)

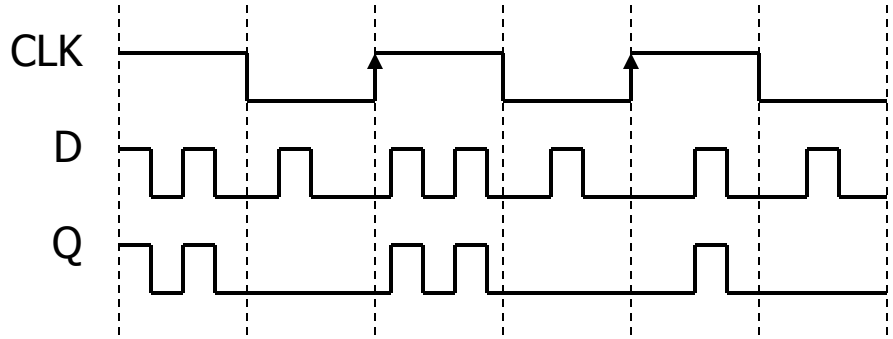
$C = 1$ means Reset



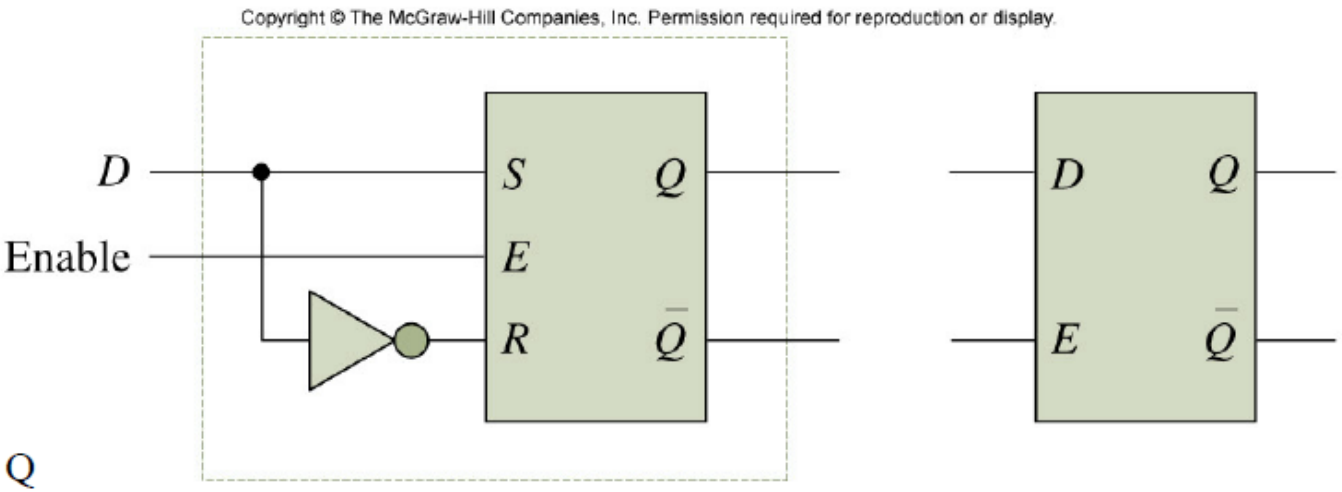
Level-Sensitive Flip-Flop

- Level-sensitive flip-flop (also called a “latch”)
- “Q” changes whenever clock is “high”

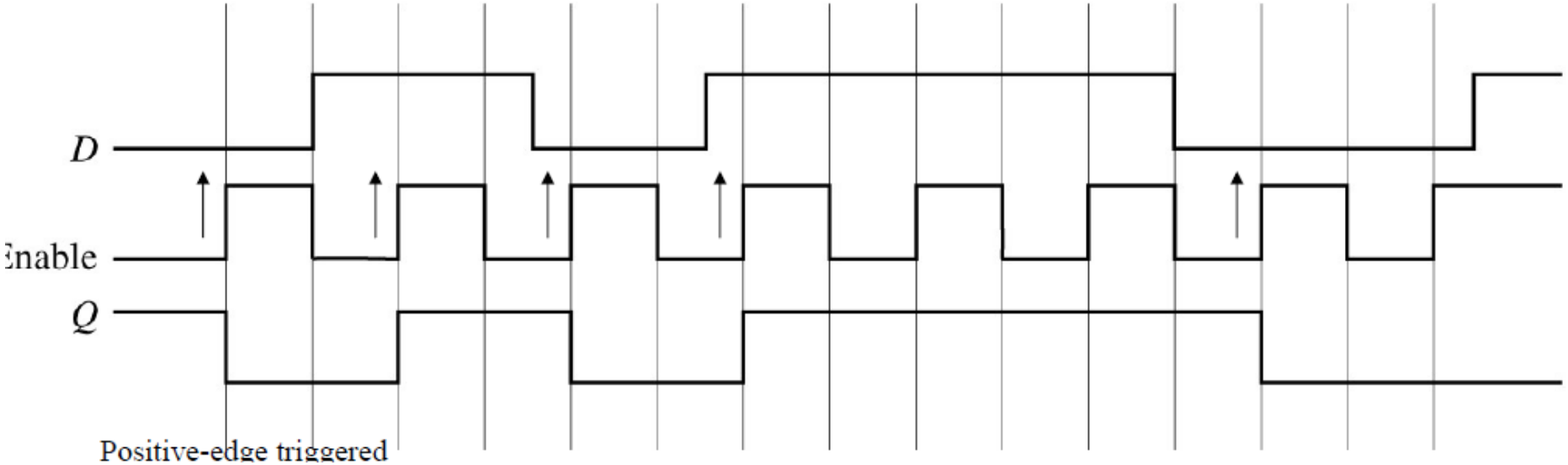




D Flip Flop

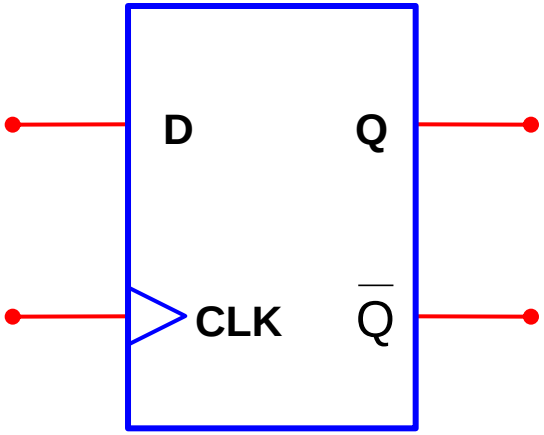


D	CLK	Q
0	↑	0
1	↑	1



Positive-edge triggered

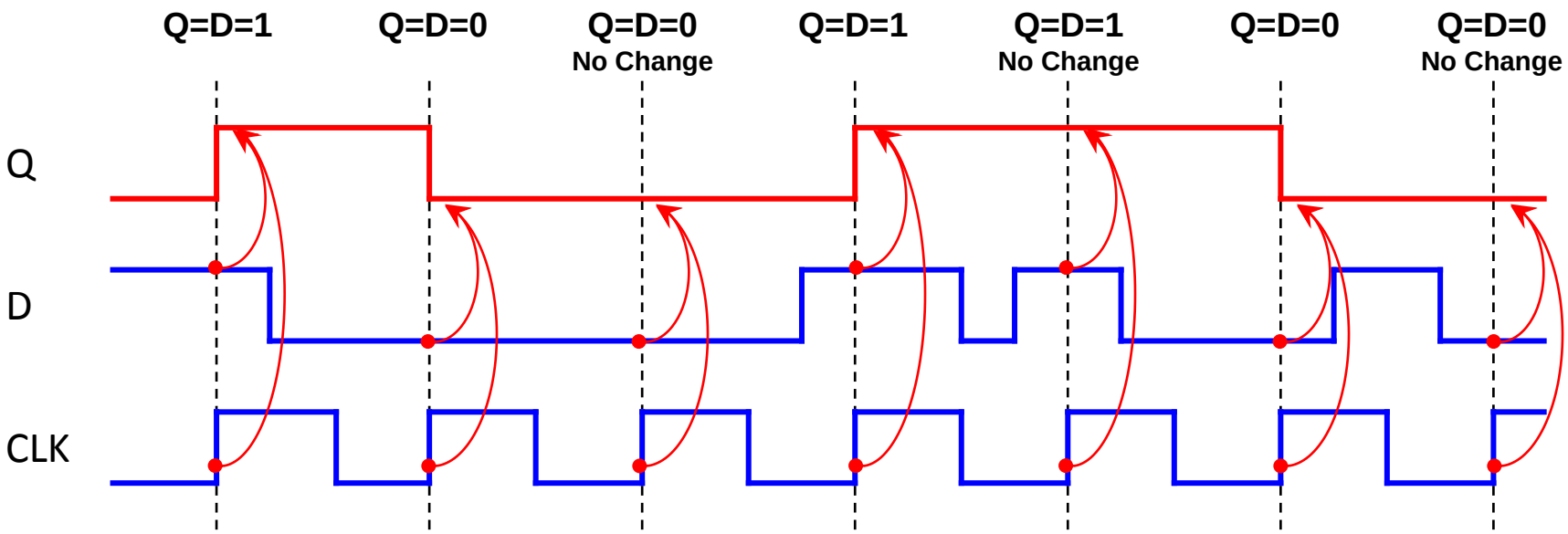
D Flip-Flop: Excitation Table



D	CLK	Q	$\overline{Q}$
0	↑	0	1
1	↑	1	0

↑ : Rising Edge of Clock

Timing of D Flip-Flop



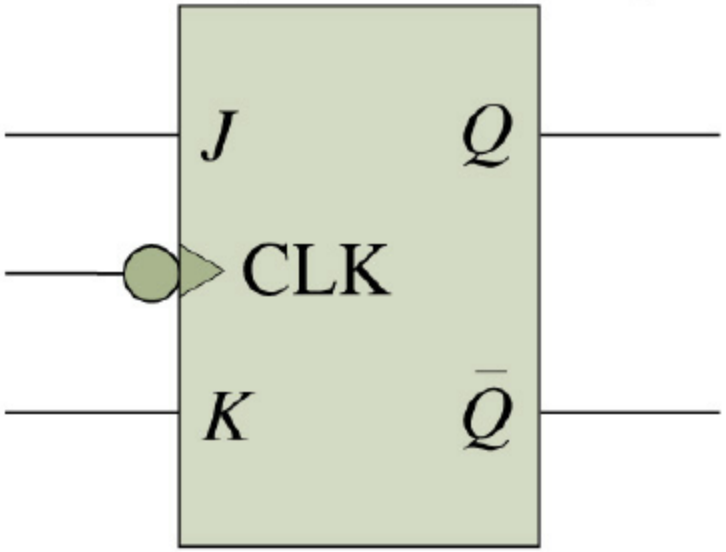
If one input (J or K) is at logic 0, and the other is at logic 1, then the output is set or reset (by J and K respectively), just like the RS flip-flop, but on the (falling) clock edge.

If both inputs are 0, then it remains in the same state as it was before the clock pulse occurred; again like the RS flip flop.

If both inputs are high, however the flip-flop changes state whenever the (falling) edge of a clock pulse occurs; i.e., the clock pulse toggles the flip-flop.

See to the right

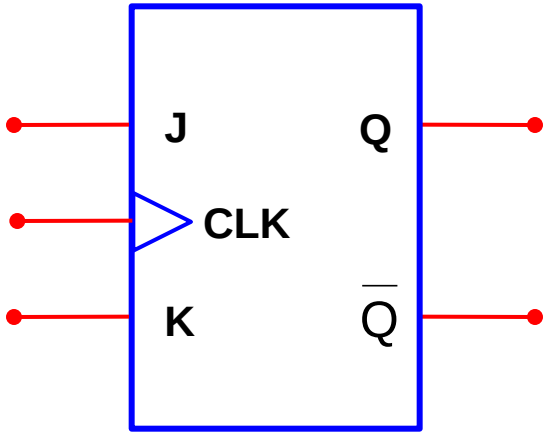
Truth table for the *JK* flip-flop



JK flip-flop

J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0 (reset)
1	0	1 (set)
1	1	$\bar{Q}_n$ (toggle)

J/K Flip-Flop: Excitation Table

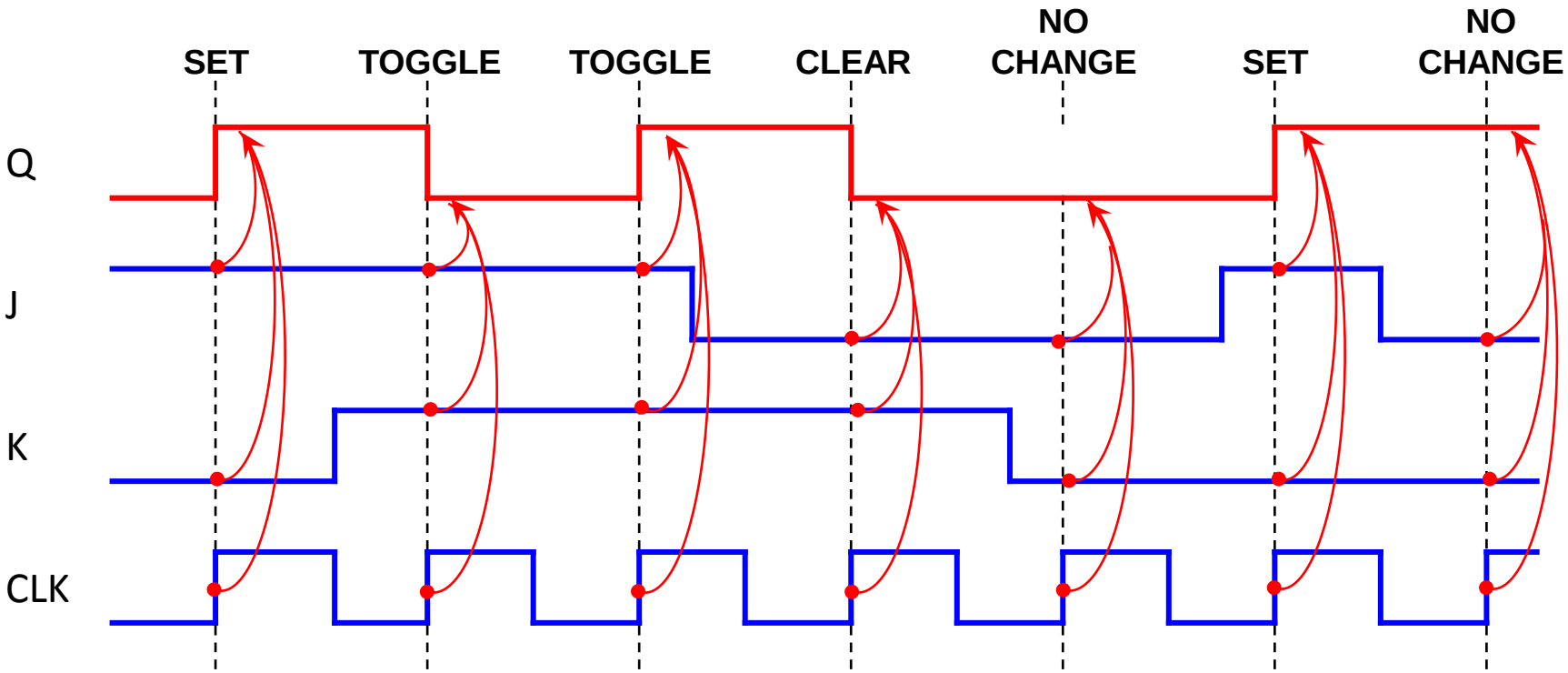


J	K	CLK	Q	
0	0	↑	Q_0	No Change
0	1	↑	0	Clear
1	0	↑	1	Set
1	1	↑	$\overline{Q}_0$	Toggle

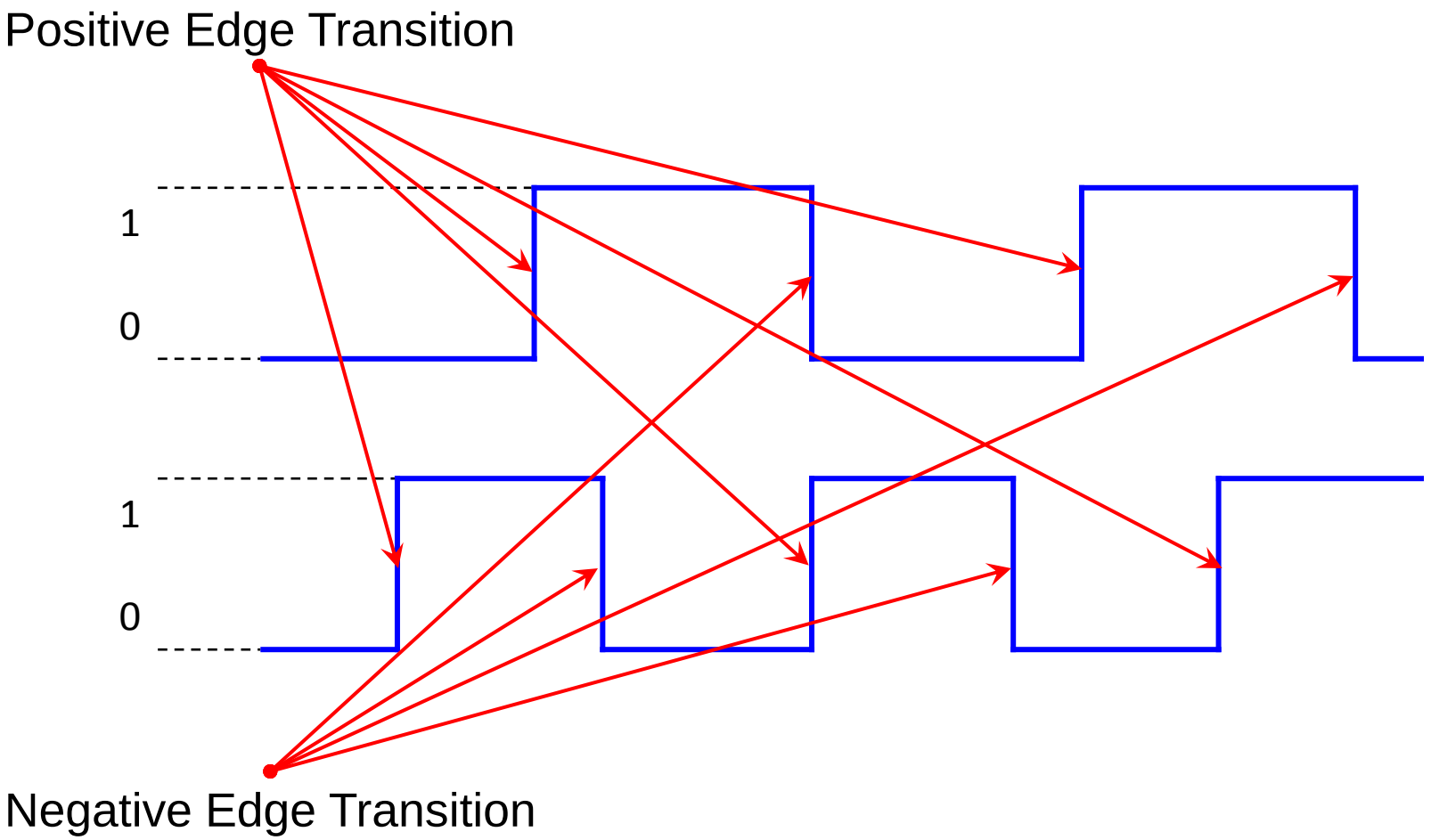
↑ : Rising Edge of Clock

$\overline{Q}$: Complementof Q

J/K Flip-Flop: Example Timing

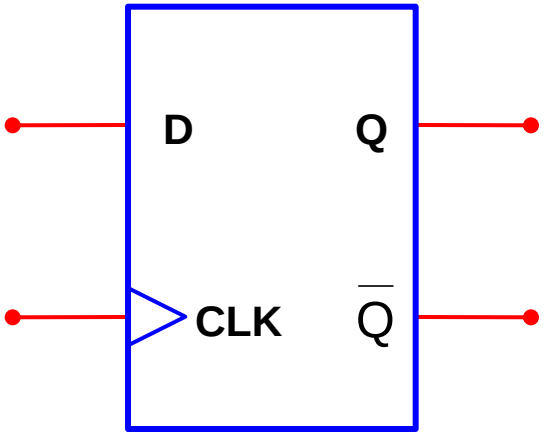


Clock Edges



Positive and Negative Edge Triggered D

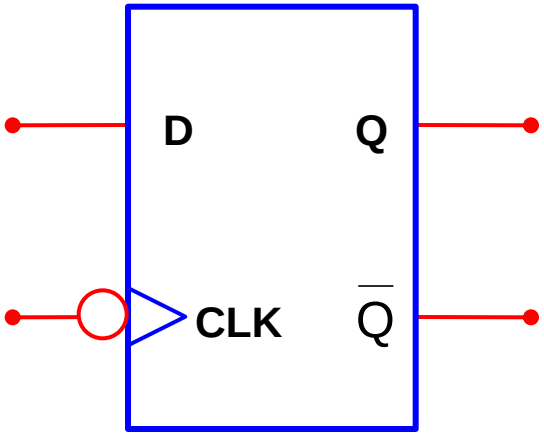
Positive Edge Trigger



D	CLK	Q	$\overline{Q}$
0	↑	0	1
1	↑	1	0

↑ : Rising Edge of Clock

Negative Edge Trigger

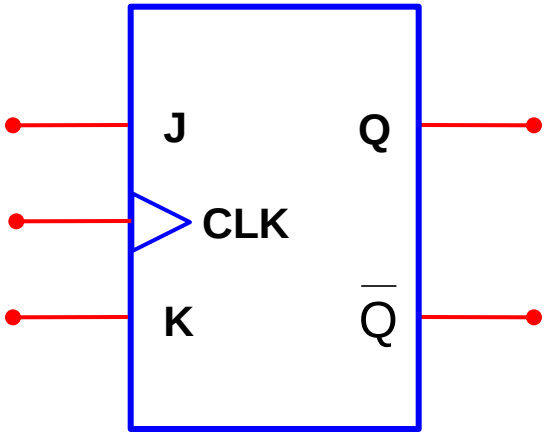


D	CLK	Q	$\overline{Q}$
0	↓	0	1
1	↓	1	0

↓ : Falling Edge of Clock

Edge Triggered J/K

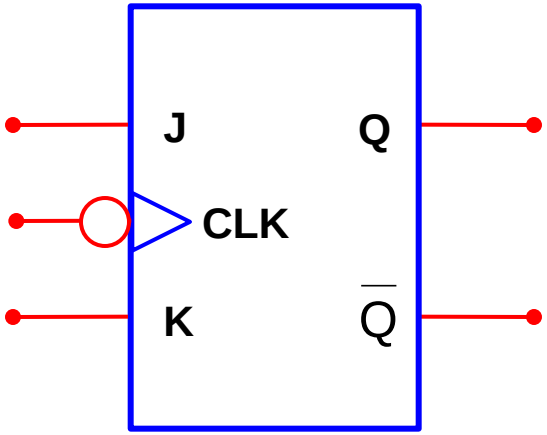
Positive Edge Trigger



J	K	CLK	Q
0	0	↑	Q_0
0	1	↑	0
1	0	↑	1
1	1	↑	$\overline{Q}_0$

↑ : Rising Edge of Clock

Negative Edge Trigger



J	K	CLK	Q
0	0	↓	Q_0
0	1	↓	0
1	0	↓	1
1	1	↓	$\overline{Q}_0$

↓ : Rising Edge of Clock

Flip-Flop Versus Latch

- The primary difference between a D flip-flop and D latch is the EN/CLOCK input.
- The flip-flop's CLOCK input is edge sensitive, meaning the flip-flop's output changes on the edge (rising or falling) of the CLOCK input.
- The latch's EN input is level sensitive, meaning the latch's output changes on the level (high or low) of the EN input.